REMARKS

Applicants appreciate the examination of the present application that is evidenced by the Official Action of January 30, 2008. Nonetheless, Applicants respectfully request reconsideration of the outstanding rejections based on 35 USC § 102. In particular, Applicants respectfully request reconsideration of the outstanding rejections based on Forrest et al., because Forrest et al. merely discloses a one-time programmable electronic memory element that utilizes a change in electrical conductivity (i.e., resistance) to set a logic 1 (or logic 0) state. As described at Col. 4, lines 13-32, of Forrest et al., the application of "a relatively high voltage pulse that irreversibly increases [the] electrical resistance" of the intersection volume of PEDT/PSS **210** of FIG. 2D, switches the logic state of a respective one-time programmable memory element from a logic 0 (or logic 1) value to a logic 1 (or logic 0) value. This change in electrical resistance of a memory element during a one-time programming operation results in a change in the magnitude of the current that passes through the memory element during an operation to read the value of the data "stored" within the memory element:

> ".... As shown in FIG. 2D, the volume of PEDT/PSS **210** overlying the first signal line **202** and underlying the second signal line **208** within the overlap region of the two signal lines **202** and **208**, along with the two signal lines **202** and **208**, constitutes a memory element. It is this intersection volume **210**, along with an additional volume of the PEDT/PSS layer surrounding the intersection volume **210**, through which current is conductive when a voltage differential is applied to the two signal lines." (Forrest et al., Col. 3, lines 53-62).

Thus, as clearly stated by Forrest et al., the application of a "high voltage pulse" across the memory element **210** operates to program the memory element **210** from a relatively highly conductive "post fabrication state" to a relatively highly resistive state. This programming operation is "irreversible." (See, Forrest et al.,

Col. 4, lines 20-21). An operation to "read" the programming state of the memory element **210** is performed by detecting a magnitude of the current passing through the memory element **210**:

> ".... However, the PEDT/PSS layer between the two metallic conductive elements can be subjected to a relatively high voltage pulse to be irreversibly switched to a much less conductive state. Both states are stable when subjected to relatively low-voltage currents that can be employed to [read] the state of the memory element." (Forrest et al., Col. 3, lines 7-13, underlining added).

These disclosures of Forrest et al. demonstrate that the memory element **210** can only be irreversibly programmed (i.e., one-time programmable – "write once read many times" (WORM)) and, once programmed, can be "read" by measuring a magnitude of a current passing through the signal lines **202** and **208** and the memory element **210**. Applicants submit, however, that these disclosures of Forrest et al., are in stark contrast to the claimed subject matter of the present application, which recites a "reversibly switchable" memory element that stores data in the form of an "optical state" – not an electronic state (i.e., resistance). The optical states are determined by the optical characteristics of "rotatable molecular components" **108** illustrated by FIGS. 1-2 of the present application, which are set by opposing electric fields **110** (in FIG. 1) and **202** (in FIG. 2). Accordingly, whereas the claimed invention is directed to memory cells that may be repeatedly programmed (and erased) and store data as an optical characteristic (i.e., rotation of the circular components **108**), the memory elements of Forrest et al. can only be programmed one time (i.e., the programmed state is "irreversible") and store data as an electrical characteristic (i.e., resistance (high or low)). These distinctions are highlighted by each of the independent Claims 1, 6, 12 and 16. Applicants submit, therefore, that all of the pending Claims 1-20

are patentable over Forrest et al. and the other cited prior art references.

Applicants have also addressed the section 112 rejections to Claims 17-20.

Respectfully submitted,

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